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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,826	FENG, KAI D.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,14-18 and 20-23* is/are rejected.

7)☒ Claim(s) *5-13,19 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/3/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1- are rejected under 35 U.S.C. 102(e) as being anticipated by Funaba (6,853,213).

Funaba shows:

1. a simultaneous bi-directional data bus (DQn, Fig. 7) comprising:

a simultaneous bi-directional data bus (DQ) having a characteristic impedance Z0;

a first driver unit (101) and receiver unit (111) connected to a first terminal end of the simultaneous bi-directional data bus;

a second driver unit (201) and receiver unit (211) connected to a second terminal end of the simultaneous bi-directional data bus;

each of the first driver unit and the second driver unit having a sourcing current source (MP11 & R11, Fig. 1) and a first resistor (R13) connected in parallel between a voltage supply and a terminal end of the simultaneous bi-directional data bus, and a

sinking current source (R12 & MN11) and a second resistor (R14) connected in parallel between a ground and a terminal end of the simultaneous bi-directional data bus, wherein a substantially higher impedance of each current source relative to a substantially lower impedance of each resistor connected in parallel to the current source (the impedance combination of MP11 and R11 is higher than R13 alone) provides a relatively constant impedance in each driver unit which substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

2. The simultaneous bi-directional data bus of claim 1 where, in each of the first driver unit and the second driver unit, the first resistor of the sourcing current source and the second resistor of the sinking current source is substantially equal to twice the characteristic impedance of the simultaneous bi-directional data bus (100 ohms, col. 9, line 18-19).

3. The simultaneous bi-directional data bus of claim 1, wherein the sourcing current sources of each of the first driver unit and the second driver unit are identical sourcing current sources, and the sinking current sources of each of the first driver unit and the second driver unit are identical sinking current sources (col. 7, lines 56-59).

4. The simultaneous bi-directional data bus of claim 1, wherein each driver unit comprises a p side driver (MP11-MP12) and an n side driver (MN11-MN12) which are serially connected between a voltage supply and ground, with the connection between the serially connected drivers being connected to the simultaneous bi-directional data bus, and each driver unit has an output impedance of substantially twice the characteristic impedance (100 ohms) of the simultaneous bi-directional data bus so that

the total output impedance of each driver unit substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

The limitations of claims 15-18 are rejected as above; furthermore, Funaba shows a second driver unit (102) and receiver unit (112) connected to a second terminal (DQ2) end of the simultaneous bi-directional data bus. The rest see figures 1-3.

The apparatus described above is applicable to the method claims 20-23.

Allowable Subject Matter

3. Claims 5-14, 19, 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Sundstron (5,602,494) shows an Bi-direction programmable I/O circuit having resistors in parallel with transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

4/11/05